Author Accepted Manuscript (AAM)
the final version is published on IEEE Xplore as follows: https://ieeexplore.ieee.org/abstract/document/11222503
DOI: 10.23919/EMPC63132.2025.11222503

A Study of 355 nm UV Laser Ablation Process For Singulation of Silicon Wafers

Serguei Stoukatch
Microsys lab, Department of Electrical Engineering and Computer Science
Liege University
Liege, Belgium
serguei.stoukatch@uliege.be

Francois Dupont
Microsys lab, Department of Electrical Engineering and Computer Science
Liege University
Liege, Belgium
fff.dupont@uliege.be

Jean-Michel Redouté
Microsys lab, Department of Electrical Engineering and Computer Science
Liege University
Liege, Belgium
jean-michel.redoute@uliege.be

***Abstract*— This work presents the results of the development of a 355 nm nano-second UV laser ablation process for silicon wafer singulation. The study focuses on the two most prevalent crystal orientations in semiconductor manufacturing: Si (100) and Si (111). The developed laser ablation process is purely dry, doesn't require any liquid, vapor phase or plasma and minimizes particles generation in the close vicinity of the dicing street. This process is specifically suitable for applications involving wafers sensitive to liquid exposure and particles contamination. Notable examples include MEMS devices and metal-oxide (MOX) micro-hotplate gas analyzers, where conventional blade dicing with constant water flow may cause irreversible damage to delicate structures and functionalized layers, as well as introduce contamination. The proposed alternative - UV laser ablation singulation technique achieved a narrow 36 µm kerf width on 525 ± 25 µm thick Si (100) and Si (111) wafers. The process achieved an aspect ratio (cutting depth to kerf width) of approximately 15:1. Notably, no chipping on the face and backside of the wafer were observed. Furthermore, despite inherent variations in laser-ablated groove depth, cutting performance showed no statistically significant difference between Si (100) and Si (111) wafers.**

Keywords—UV nano-second laser ablation, silicon wafer ablation, metal-oxide sensor assembly, dry wafer singulation method, advance packaging, back-end processing of functionalized wafers.

I. Introduction

Mechanical saw dicing remains the dominant technology for large-scale wafer singulation in the semiconductor industry[1]. The process is highly automated and achieves high throughput, with an optimized feeding speed typically ranging from 50 to 250 mm/s [2]. Singulation of a 300 mm wafer into individual 5 × 5 mm² dies typically takes 6–10 minutes, depending on the dicing machine's speed and handling efficiency. The most common dicing process is typically used for standard wafer thicknesses of 300–500 µm. For ICs, MEMS, and sensors, this process requires a dicing street width of 50–100 µm, necessitating blades with a thickness of 40–50 µm. Ultra-thin wafers (<100 µm), designed for a 20–50 µm kerf width, require state-of-the-art dicing blades as thin as 15 µm [3]. Chipping is minimal but occurs on both the front and backside of the wafer, with backside chipping being more critical [4]. For standard silicon wafer dicing, backside chipping typically ranges from 10–50 µm [5], depending on wafer thickness [6] and process control. For advanced CMOS nodes (e.g., <100 µm wafers), keeping chipping <20 µm is critical [7].

To minimize chipping, saw dicing can be combined with laser grooving [8]. In this hybrid approach, a laser first creates a wider groove along the dicing street, after which the dicing blade completes the through-cut. However this approach doesn't eliminate the backside chipping.

Beyond chipping concerns, conventional saw dicing is not a dry process - it requires water for cooling rotating blades and removing silicon dust. However, there is growing demand for dry processing, particularly for moisture and dust sensitive applications like certain MEMS and MOX gas analyzers [9] where the workpiece cannot be exposed to water, other liquids, vapors, or plasma phases. Currently, few viable alternatives [10] meet these stringent requirements. Among the available options, laser ablation and stealth dicing techniques show the most promise. The application of laser ablation for silicon wafer singulation has been widely studied, as evidenced by numerous publications in this field. Comprehensive reviews of laser-based singulation methods [11] provide detailed analyses of various approaches, including comparative studies of UV laser technologies [12] for wafer processing applications. However, due to several reasons such throughput limitations, high equipment cost, thermal damage risks, industry inertia and process maturity, laser dicing is not extensively used for cutting silicon wafers at present. Currently laser ablation dicing is adopted for thin wafers (<100 µm), and ICs with ultra-low chipping requirements [13]. Stealth dicing dominates for MEMS, image sensors [14]. The ablation laser dicing process for singulation of silicon wafers requires further in-depth research. A comparative analysis of the processes of saw cutting and laser ablation is presented in Table I.

TABLE I. SAW DICING PROCESS COMPARED WITH LASER ABLATION

Factor	Saw Dicing	Laser ablation
Process maturity	High	Low
Speed	High	Slow
Process cost	Low	High
Chipping	10-50 µm	<10 µm or none
Contamination	Present	Limited*
Dry process	No, requires water	Yes, dry
Thermal damage	None	Limited*

*Must be investigated.

This paper is organized as follows: The Introduction section examines viable alternatives to conventional saw dicing that meet stringent dry processing requirements. Section II describes the materials and methods used in our study, with particular emphasis on silicon crystal orientation and its potential impact on processing outcomes. Section III presents and analyzes the experimental results. Finally,

Funded by the European Union. GA nr. 101130159, AMUSENS project.

conclusions and future research directions are provided in Section IV.

II. Materials and Methods

A. Siclicone wafer consideration

Silicon has a diamond cubic crystal structure, and its orientation is defined using Miller indices, such as (100), (110), and (111) [15]. The difference in crystal orientation among Si (100), Si (110), and Si (111) wafers arises from their crystalline structure, as different orientation planes exhibit varying atomic densities and bond strengths [15]. Si (100) contains planes with atoms spaced farther apart, whereas Si (111) has densely packed planes with stronger bonds. Si (110) presents intermediate state between (100) and (111) in terms of atomic density. The Si crystal orientation has an effect on material properties. The etch rates of silicon depend on the crystallographic orientation [16]. Wet etching of silicon is highly anisotropic due to differences in atomic packing densities between planes. Si (111), due to higher atomic density and stronger bonds, etches much slower than Si (100) in potassium hydroxide (KOH) (50 times slower) and tetramethylammonium hydroxide (TMAH) (50 times slower) [17]. Whereas HF/HNO_3 mixtures etch isotropically Si (100) and Si (111) with rate of 1 to 50 µm/min with no crystal orientation dependence [18]. Dry etching [19] (e.g., reactive ion etch (RIE), deep reactive ion etch (DRIE, known also as Bosch process) is less orientation-dependent than wet etching but can still show slight variations due to ion bombardment and passivation effects. Si (111) etches about 10% slowly by RIE and DRIE [20]. There are several other specificities for Si (111) and Si (100) that must be taken into account [21]. Si (111) is more expensive compared to Si (100) [22]. The Si (111) surface is superior for advanced CMOS technology nodes because it is more dense [23]. Si (111) has lower surface state defect density. Surfaces Si (100) tends to be flatter and smoother and exhibits hydrophobic properties, facilitating dopamine and oxide growth. Whereas Si (111) has lower oxide growth rate. Si (111) wafers cleave more easily than Si (100) due to their crystal structure because its different cleavage planes and surface energy due to crystal orientation [21, 24]. As a result of that Si (111) typically produces smoother, mirror-like cleaved edges with minimal force. For this study, we used silicon wafers with the two most common crystal orientations in semiconductor manufacturing: Si (100) and Si (111) [15, 25]. Si (100) is typically used for CMOS integrated circuits (IC) and dominated CMOS logic ICs, flash memory. DRAM and SRAM manufacturing are also shifted to (100) orientation for better wafer flatness and enables smaller features sizes. While Si (111) is commonly employed in MEMS devices, LEDs, and epitaxial growth (e.g., III-V materials). A summary of basic characteristics of silicone substrates depending on crystallographic orientation are presented in Table II.

TABLE II. Comparision of basic Silicon characteristics

Factor	Si (100)	Si (111)
Process maturity	High	Medium
Cost	Low	High
Atom density	Low	High
Wet etch	High	Slow
Dry etch	Average	Average, 10% slower
Cleaving	Difficult	OK
Applications	CMOS, MEMS	MEMS, LED, epitaxy Advanced CMOS node

While Si (110) [26] is a less common silicon wafer orientation, its asymmetric surface structure offers distinct advantages for specialized applications requiring anisotropic etching or tailored electronic properties. As a result, it is used only where these specific properties are essential—such as in MEMS devices, heterojunction bipolar transistors, certain power electronics, and heteroepitaxial growth (e.g., GaN or SiGe on Si).

The study was carried out on a polished silicon wafer with a diameter of 100 mm, a standard thickness of 525 ± 25µm, and a total thickness variation (TTV) < 5 µm. The wafer with crystal orientation Si (111) is N-type, dopant As, Czochralski method (CZ), and a resistivity of 0.0020–0.0045 Ohm.cm. The wafer Si (100) is P-type, dopant B, CZ and a resistivity of 1–5 Ohm.cm.

The laser ablation is a photochemical etching process that started on the wafer surface and progress sequentially into wafer's depth till it reach the wafer backside, wherefore we might expect that the crystal orientation might have an effect on the laser ablation process. However we did not find conclusive data on this topic. As wet and dry etching rates vary considerably with different crystal planes, one can expect impact of Si crystal orientation on the laser ablation rate and the laser cut or silicon kerf characteristics.

B. Instrumentation

We performed the study using a WS Flex optomechanical system from Optec, Belgium. It is equipped with a nano-second Talon 355-12 W (Spectra Physics, USA) 12 W Nb: YAG Q-switched DPSS laser, with a wavelength of 355 nm (UV) [27]. The laser beam spot size diameter at target is 8 µm at waist. The pulse width is <25 ns at 100 kHz.

The laser system has different options to hold the work piece during processing. In this study we used a porous ceramic workpiece holding system with holding area dimensions of 300 x 220 mm. The porous ceramic plate (sintered ceramic, METAPOR CEl00 White, sourced from Portec AG, Switzerland, and manufactured by Horst Witte, Germany and designed by Optec) has pore size of 10-12 µm and porosity value of 20%, with flatness better than of 20 µm. The ceramic plate secures the Si wafer without displacement during the entire processing.

The laser has several parameters that can be adjusted within the operating range (laser repetition rate, laser spot speed, laser pulse energy, number of repetitions, etc.), however some of them are interdependent. We adjusted the laser speed to obtain a 50% diameter overlap between successive laser spots, as well as other parameters to obtain maximum laser fluence [28, 29]. The laser power was adjusted to the maximum to increase the process speed. For that we used a maximum diode current of 7.26 A and optimized combination of other variable such as spot speed, repetition rate. The variable parameter during the study was the number passes or repetitions, which is the number of times the laser beam moves through the programmed pattern.

For all optical observation in visible light range, reflective view, we used Leica Z6APO optical microscope, with a magnification to from 7^x to 225^x.

III. Results and Discussion

A. *Determining the optimal number of laser passes required for full-thickness cutting of a silicon wafer*

On the first stage of the evaluation, we defined the number of laser passes required to perform a complete cut through a 525 ± 25 µm thick silicon wafer of Si (100) and Si (111) crystal orientations in order to detect the difference if there is any. As a test pattern, we have chosen a square pattern of 5 mm × 5 mm, which is a typical size for a silicon die or MEMS device.

The wafer was placed of the work holder of the laser system and firmly secured using the porous ceramic holding system by vacuum. On this stage of development, we did not mount the wafer on the dicing tape, which is commonly used for dicing processes, such as sawing by rotating blade. This is necessary to avoid interaction between the wafer and the dicing tape, which could lead to contamination of the wafer with decomposition products of the dicing tape. The dicing tape is typically soften already at temperature 40°C and above. For example the most common dicing tape, is Nitto dicing tape V8A [30] (so-called a "blue" dicing tape), is polyvinyl chloride (PVC) based. PVC has a glass transition temperature of 80°C, and melting point of 100°C. Whereas the melting point of silicon is 1414 °C, that is, an order of magnitude higher than that of PVC. The risk is that the PVC will start to melt due to heat transfer from the top side of the wafer to the back. After the laser beam cuts through the wafer, it will reach the tape and due to the high fluence, it will easily decompose the dicing tape causing unwanted contamination of the wafer. On each silicon wafer Si (111) and Si (100), we processed the square pattern of 5 × 5 mm^2 using variable number of laser passes starting from 1 to 1000 as follows (0, 10, 20, 50, 100, 500, 1000) and observed the number of passes required to cut the wafer through. Appling 1000 or more repetitions resulted a complete cut of a 525 ± 25 µm thick silicon wafer. Then we studied the process window between 500 and 1000 passes with step of 100, and then between 600 and 800 with step of 25 passes. We observed two regimes: the first one is from 625 to 725 passes, after which the wafer looks cut through, however to release the die it is necessary to apply an external force from the backside of the die to eject the die. The second regime starts from 750 repetition, when the cut die is released from the wafer without an external force. We found no difference in the number repetition to cut through Si (111) and Si (100) wafers.

In principle, die ejection by external force is an acceptable process step and is a common and highly automated process in which each individual die, separated for example by saw cutting, is ejected from the cutting tape, then picked and placed in a designated assembly location or in the die trey. The issue here that in our case, we die needs ejection because it did not cut through and remains attached to the wafer. The ejection breaks whose uncut area and created unwanted chipping on the die side wall and die backside. Therefor, 750 passed must be applied in order to cut and release each individual die. Performing 750 laser passes on a 5 × 5 mm^2 square pattern requires 111 seconds for 525 ± 25 µm thick silicon wafers of Si (100) and Si (111) crystal orientations.

B. *Relationship between laser cut depth and the number of laser passes.*

As we previously found that 750 laser passes are required to cut through of 525 ± 25 µm thick silicon wafers, we would like to get the accurate value of the laser cut depth as a function of the number of the laser passes for both silicon wafers of Si (100) and Si (111) crystal orientations and to detect the difference if there is any. For that we set up the experiment as follows, first we singulated each wafer of Si (111) and Si (100) on the individual dies of 5 × 5 mm^2 using 750 laser passes, and then within each die we ablated a square pattern of 2 × 2 mm^2, which is a typical size for a small IC die, MEMS and MOX-gas analyzes. The square patterns of 2 × 2 mm^2 were processed using variable number of laser passes starting from 1 to 650 (1, 10, 50, 100, 200, 300, 400, 500, 600 and 650 passes). The photograph of the 5 × 5 mm^2 with the 2 × 2 mm^2 pattern processed is presented in the fig. 1.

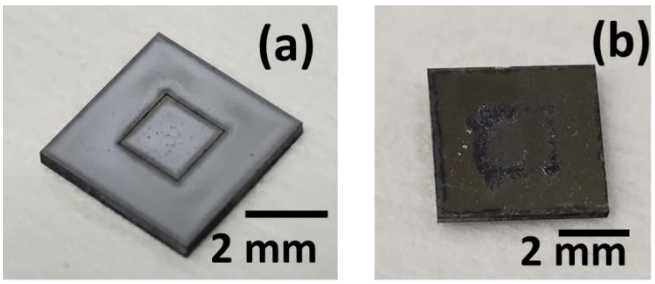

Fig. 1. The photograph of the 5 × 5 mm^2 with the 2 × 2 mm^2 pattern processed, where a). front perspective view of the die, and b). backside view.

We analyzed processed samples using a cross-sectioning method. The method is destructive and can help to observe the laser groove appearance, to characterize its depth and width, and eventually to detect various latent defects and irregularities related to the laser ablation and die release processes. The cross-sectioning method includes the sample preparation and samples characterization using an optical inspection. In order to protect the fine and brittle laser groove from eventual damage caused by the polishing, we applied on each individual laser groove an thin layer (about 200 µm thick) of underfill material. The underfill is a low viscosity epoxy compound that typically used for underfilling application. For that, we selected the underfill LOCTITE ECCOBOND E 1172 A, from Henkel [31] with viscosity of 17,000 mPa·s and maximum particle size of 20 µm that lets to fill in gap as small as 25 µm. After that, each individual die was embedded in a molding compound for an accurate handling. Then, each die was by sequential polishing using abrasive paper set of different grids (starting from #320 to #4000) and finished it with a final polish using diamond suspension of 0.5 µm diameter on a soft polishing cloth. The fig. 2 presents cross-sectioning direction and position of the 5 × 5 mm^2 die.

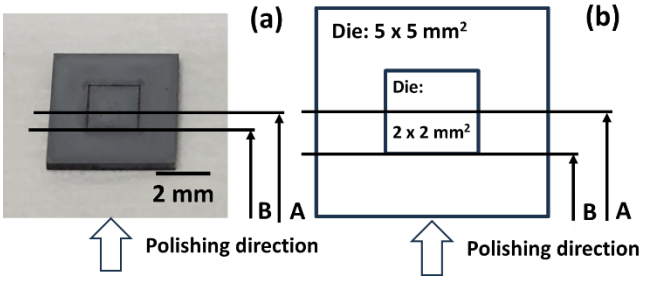

Fig. 2. Direction and position of cross-sectioning on the 5 × 5 mm2 die.

The cross-sectioning images of the 5 × 5 mm^2 die processed on Si (100) and Si (111) wafers using various

number laser passes observed at cut line A are presented in the fig. 3 and fig. 4 correspondingly.

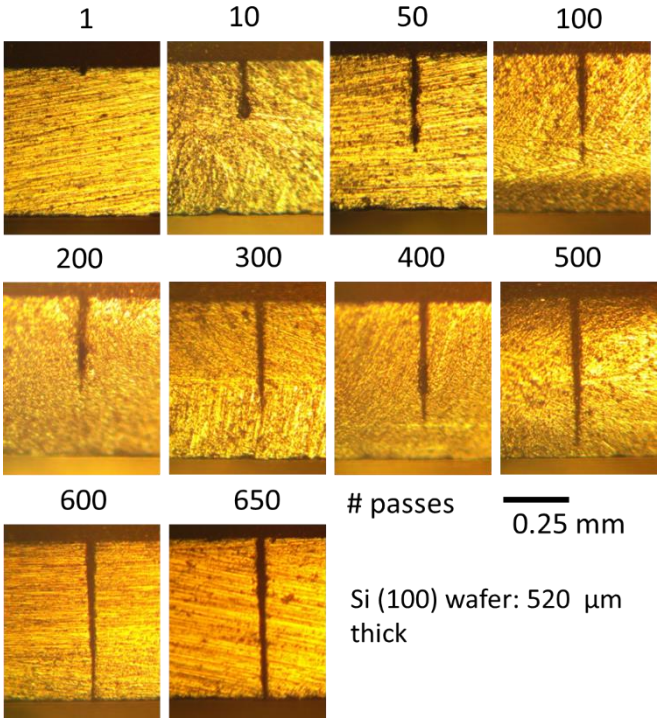

Fig. 3. Silicon wafer of Si (100): Cross-sectional view of the laser cut. Numbers on top of an individual image represents number laser passes.

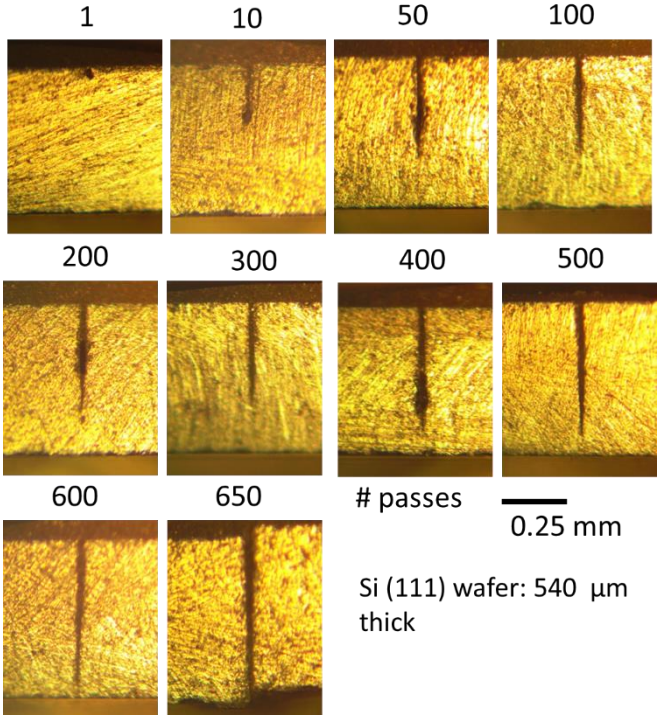

Fig. 4. Silicon wafer of Si (111): Cross-sectional view of the laser cut. Numbers on top of an individual image represents number laser passes.

Using the optical microscope Leica Z6APO we observed and measured the laser groove depth and groove diameter at the top and the bottom of the groove. The results of the laser groove depth versus the number laser passes for the silicon wafers of Si (111) and Si (100) are presented in the fig. 5.

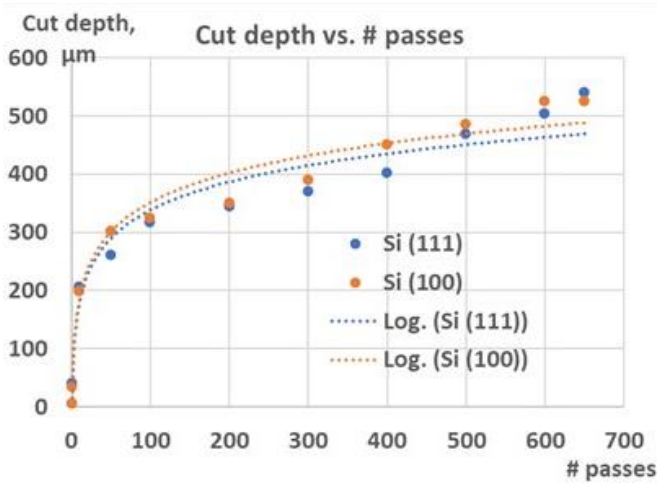

Fig. 5. The laser groove depth on Si (100) and Si (111) as a function of number laser passes (from 1 to 650 passes). The trendline is drawn using logarithmic approximation.

The laser groove depth versus number laser passes is not linear. A single laser pass produces a groove with an initial depth of 30–40 µm, after which the depth increases rapidly with subsequent passes. Notably, just 100 laser passes suffice to achieve a 320 µm deep cut in silicon, exceeding half the wafer's total thickness (525 ± 25 µm), with a total processing time of only 12.5 seconds. Subsequently, the cutting speed decreases and stabilizes at approximately 0.36 µm per laser pass. Fig. 5 suggests that 50 to 600 passes produce deeper grooves in the Si (100) wafer, though the depth difference does not exceed 50 µm.

In addition to cross-sectioning the sample along line A, we also analyzed selected samples along line B. Unlike line A, which contains two grooves, line B includes an additional groove oriented perpendicular to these. The results are presented in fig. 6.

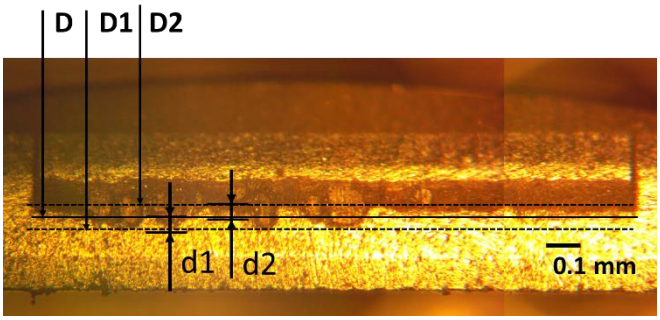

Fig. 6. Cross-sectional view of the laser cut along line B. Where *D* is the average depth of the groove, *D1* is the deepest point of the groove and *D2* is the highest point of the groove; *d1* and *d2* are the diviation from the average depth to the upper and the lowest point of the groove, respectively.

The deviation from average depth was measured on selected samples, and *d1* and *d2* has almost the same value and ranges from 20 to 35 µm. This means that the groove depth variation is in the range of 40 to 70 µm. There may be several reasons for this groove depth variation. The investigated wafers have TTV < 5 µm, the porous ceramic plate that holds the wafers during laser ablation with pore size of 10-12 µm, with flatness better than of 20 µm can also contribute to this. In addition, we don't know how intrinsically flat the laser cut is [32]. Due to variations in laser-ablated groove depth, we find no significant difference in cutting performance between Si (100) and Si (111) wafers.

C. Laser cutting width along the wafer depth.

We measured the laser cutting width on top of the die and at the deepest point of the laser groove. The typical cross-sectioning view used for characterization is presented in the fig. 7.

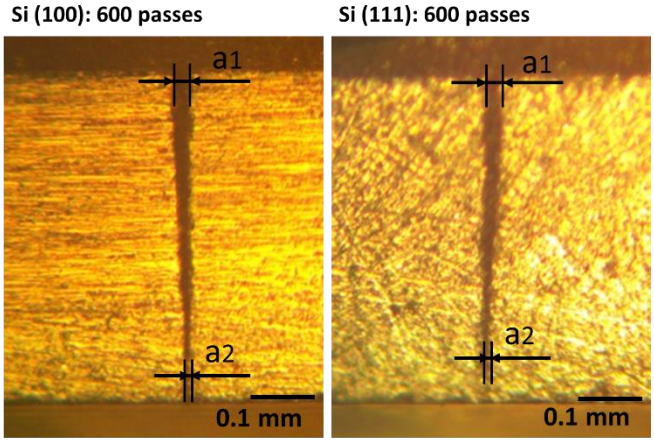

Fig. 7. Cross-sectional view of the laser cut performed on the Si (100) and Si (111) using 600 passes. Where *a1* is the width of the groove at the top of the die, and *a2* is the width of the groove at deepest point.

The data on the laser cutting width on top of the die (*a1*) and at the deepest point of the laser groove (*a2*) in function of number of the laser passes are presented in the table III.

TABLE III. LASER CUTIING WIDTH ALONG THE SI (100) AND SI (111) WAFER DEPTH

# passes	Si (100)		Si (111)	
	Top: a1, µm	*Bottom: a2, µm*	*Top: a1, µm*	*Bottom: a2, µm*
01	34.01	16.71	32.99	18.65
10	34.44	12.67	34.01	15.78
50	32.51	12.89	35.86	11.05
100	33.34	14.86	34.81	11.51
200	35.38	11.99	34.90	11.95
300	35.99	13.88	35.82	12.42
400	35.49	10.86	34.52	12.51
500	36.64	9.56	35.86	9.65
600	36.98	11.47	37.51	12.01
650	36.06	11.96	38.91*	12.10*

*The 2 × 2 mm^2 die partially separated from the 5 × 5 mm^2 core and slightly shifted.

The laser cutting width on top of the die (*a1*) is 2-3 times larger as at the deepest point (*a2*) of the laser groove. It slightly increases from 33 µm at 1 pass to 37.5 at 600-650 passes. We did not observe clear effect of silicon crystal orientation on *a1* and *a2*. For nearly cut dies (600 and 650 passes) the aspect ratio, i.e. the ratio of the cutting depth (wafer thickness) to its width (*a1*) is about 15:1, the value is high [33], that is comparable with the other common wafer singulation techniques such saw dicing. We also did not observe any chipping on the backside of the wafer and on the side walls of the laser cut [34].

IV. CONCLUSIONS

In this study we demonstrated a UV laser ablation process on silicon wafer of the two most prevalent crystal orientations in semiconductor manufacturing: Si (100) and Si (111). Using an Optec WS Flex system equipped with a nano-second Talon 355-12 W laser, we singulated a silicon wafers of 525 ± 25 µm thick on the individual dies of 5 × 5 mm^2 and 2 × 2 mm^2 . The laser-cut kerf exhibits a narrow tapered profile, measuring approximately 36 µm at the wafer face surface and narrowing to about 12 µm at the bottom. The process achieved an aspect ratio (cutting depth to kerf width) of approximately 15:1. Notably, no chipping on the face and backside of the wafer were observed. Furthermore, despite inherent variations in laser-ablated groove depth, cutting performance showed no statistically significant difference between Si (100) and Si (111) wafers. The developed laser ablation process is purely dry, doesn't require any liquid, vapor phase or plasma and minimizes particles generation in the close vicinity of the dicing street. This process is specifically suitable for applications involving wafers sensitive to liquid exposure and particles contamination.

The current laser ablation process demonstrates a throughput of 111 seconds for 5 × 5 mm² dies and 77 seconds for 2 × 2 mm² dies in 525 ± 25 µm thick silicon wafers. While this processing speed remains relatively slow, significant optimization potential exists. Further development should focus on both performance improvement and identification of fundamental physical limitations

Meanwhile we see a potential of proposed technology for cutting a thinner wafer, 300 µm and below. To achieve a cut depth of 320 µm the processing time is 12.5 seconds that can be acceptable speed for the 300 µm thick silicon wafers. The system completes 10 and 50 laser passes in just 1.9 seconds and 6.6 seconds per die respectively, achieving a cut depth of 200 µm. For shallower cuts (50-100 µm), only 5 repetitions are required, with processing times under 1 second. These promising results, however, require experimental validation on actual wafers of corresponding thicknesses.

ACKNOWLEDGMENT

The work was fully funded by the European framework program HORIZON-CL4-2023-RESILIENCE-01-33 - Smart sensors for the Electronic Appliances market (RIA), GA nr. 101130159, AMUSENS project. Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. Neither the European Union nor the granting authority can be held responsible for them.

This research paper was inspired by consortium members during the preparation and implementation of the AMUSENS project.

REFERENCES

[1] Thin Wafer Processing & Dicing Equipment Market – Forecast (2025-2031), https://www.industryarc.com/Report/17062/thin-wafer-processing-dicing-equipment-market.html?utm_source=article&utm_medium=social, &utm_campaign=Rani, Accessed on May 28, 2025.

[2] D. Li, W. Jiang, H. Qi, "Optimized for Silicon Wafer Dicing Blade Machining and Grinding Parameters of Structure", Manufacturing Technology, 25, 2025, https://doi.org/10.21062/mft.2025.009.

[3] DISCO, Dicing blades , ZH05, https://disco.co.jp/eg/products/blade/zh05.html, Accessed on May 28, 2025.

[4] Y. H. Chiew, J. Y. Liong and F. F. Tan, "Mechanical Dicing Challenges and Development on 50um Saw Street with Wafer Backside Coating (WBC)," 2018 IEEE 38th International Electronics Manufacturing Technology Conference (IEMT), Melaka, Malaysia, 2018, pp. 1-8, https://doi.org/10.1109/IEMT.2018.8511708.

[5] T.-J. Su, Y. F. Chen , J.-C. Cheng, C.-L. Chiu, “Optimizing the dicing saw parameters of 60 μm wafer dicing street”. Microsystem Technologies. 24. , 2018, https://doi.org/10.1007/s00542-017-3553-z.

[6] J. Shi, W. Liu, Zh. Chen, W. Cao, L.Zhou, “Optimization method of cutting parameters of wafer dicing saw based on orthogonal regression design. SN Appl. Sci. 4, 262, 2022, https://doi.org/10.1007/s42452-022-05146-1

[7] SEMI G39 (guidelines for wafer dicing quality).: https://www.semi.org/en/products-services/download-standards, Accessed on May 28, 2025.

[8] M. Fuegl, G. Mackh, E. Meissner and L. Frey, "Assessment of dicing induced damage and residual stress on the mechanical and electrical behavior of chips," 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2015, pp. 214-219, https://doi.org/10.1109/ECTC.2015.7159594.

[9] M. Birkholz, “Implantable Microelectronics”, 2022, https://doi.org/10.1201/9781003263265-21.

[10] S. Stoukatch, F. Dupont and J. -M. Redouté, “Advanced Wafer Singulation Techniques for Miniaturized Metal-oxide (MOX) Micro-hotplates Based Gas Analyzer”, 2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC), Berlin, Germany, 2024, pp. 1-8, https://doi.org/10.1109/ESTC60143.2024.10712018.

[11] H. Y. Zheng, X. C. Wang and Z. K. Wang, 5 - Laser dicing of silicon and electronics substrates, Editor(s): J. Lawrence, J. Pou, D.K.Y. Low, E. Toyserkani, In Woodhead Publishing Series in Welding and Other Joining Technologies, Advances in Laser Materials Processing, Woodhead Publishing, 2010, pp. 88-135, https://doi.org/10.1533/9781845699819.2.108.

[12] M. R. Marks, K.Y. Cheong, Z. Hassan, “A review of laser ablation and dicing of Si wafers”, PrecisionEngineering,73,377-408, 2022, , https://doi.org/10.1016/j.precisioneng.2021.10.001.

[13] Disco, Laser Saws, DFL7161, https://www.disco.co.jp/eg/products/laser/dfl7161.html, (Accessed on May 28, 2025).

[14] Disco, Laser Saws, DFL7341, https://www.disco.co.jp/eg/products/laser/dfl7341.html, (Accessed on May 28, 2025).

[15] M.J. Madou, “Fundamentals of Microfabrication: The Science of Miniaturization”, Second Edition (2nd ed.). CRC Press. , 2002, https://doi.org/10.1201/9781482274004

[16] S. Negi, R. Bhandari, “Silicon isotropic and anisotropic etching for MEMS applications”. Microsystem Technologies. 19., 2012, https://doi.org/10.1007/s00542-012-1552-7.

[17] M. Kramkowska, I. Zubel, “Silicon anisotropic etching in KOH and TMAH with modified surface tension”, Procedia Chemistry, Vol. 1, Is. 1, 2009, pp. 774-777, https://doi.org/10.1016/j.proche.2009.07.193.

[18] M. Shikida, K. Sato, K. Tokoro, D. Uchikawa, “Differences in anisotropic etching properties of KOH and TMAH solutions”, Sensors and Actuators A: Physical, Vol. 80, Is. 2, 2000, pp. 179-188, https://doi.org/10.1016/S0924-4247(99)00264-2.

[19] F. Laermer, S. Franssila, L. Sainiemi, K. Kolari, Chapter 16 - Deep reactive ion etching, Editor(s): M. Tilli, M. Paulasto-Krockel, M. Petzold, H. Theuss, T. Motooka, V. Lindroos, In Micro and Nano Technologies, Handbook of Silicon Based MEMS Materials and Technologies (Third Edition), Elsevier, 2020, pp. 417-446, https://doi.org/10.1016/B978-0-12-817786-0.00016-5.

[20] H.V. Jansen, M.J. Boer, S. Unnikrishnan, M. Louwerse, M. Elwenspoek, “Black silicon method X: A review on high speed and selective plasma etching of silicon with profile control: An in-depth comparison between Bosch and cryostat DRIE processes as a roadmap to next generation equipment”. Journal of Micromechanics and Microengineering. 19, 033001, 2009,. https://doi.org/10.1088/0960-1317/19/3/033001.

[21] S. Wolf, R. N. Tauber, ”Silicon Processing for the VLSI Era: Process technology”, Vol 1, pp. 960, 2000, Lattice Press, 2nd edition, https://books.google.be/books?id=ALoU0QEACAAJ

[22] Silicon wafers, https://svmi.com/products/#silicon-wafers, Accessed on May 28, 2025.

[23] D.J. Foster, “Silicon Processing: CMOS Technology”. In: Miller, L.S., Mullin, J.B. (eds) Electronic Materials. Springer, Boston, MA. 1991, https://doi.org/10.1007/978-1-4615-3818-9_13

[24] Silicon Wafer Market Monitor: https://www.semi.org/en/products-services/market-data/si-wafer-monitor, Accessed on May 28, 2025.

[25] R.C. Jaeger. “Introduction to Microelectronic Fabrication”, edited by G.W. Neudeck & R. F. Pierret. Englewood Cliffs: Prentice Hall, 2002.

[26] S. Franssila, “Introduction to microfabrication”. John Wiley & Sons; 2010, pp. 536.

[27] Spectra Physics: Products, Nanosecond Pulsed Lasers, https://www.spectra-physics.com/en/f/talon-q-switched-laser, Accessed on May 28, 2025.

[28] F. Dupont, S. Stoukatch, P. Laurent, S. Dricot, M. Kraft, 355 nm UV laser patterning and post-processing of FR4 PCB for fine pitch components integration, Optics and Lasers in Engineering, vol. 100, 2018, pp. 186-194.; , https://doi.org/10.1016/j.optlaseng.2017.08.014.

[29] F. Dupont, S. Stoukatch, P. Laurent, and J.-M. Redouté. "Fine pitch features laser direct patterning on flexible printed circuit board." Optics and Lasers in Engineering, vol. 126, 2020, , https://doi.org/10.1016/j.optlaseng.2019.105869

[30] Nitto, Products, Semiconductor Manufacturing Process Products, Dicing tape, V8A, https://form.nitto.com/tw/en/products/semicon/dicing019/, Accessed on May 28, 2025.

[31] Henkel Adhesives, https://www.henkel-adhesives.com/be/en/product/underfills/loctite_eccobonde1172a0.html, Accessed on May 28, 2025.

[32] H. Cao, Y. Li, G. Wang, Z. Tang, D. Sun, H. Yin, Y. Yu, Ch. Shen, Y. Wang, Zh. Lu, „Laser dicing of semiconductor wafers: Research status and current challenges”, Optics and Lasers in Engineering, Volume 186, 108786, 2025, https://doi.org/10.1016/j.optlaseng.2024.108786.

[33] Pachkawade, V., Cerica, D., Dricot, S., Stoukatch, S., Kraft, M.: Direct laser writing to fabricate capacitively transduced resonating sensor, Microsystem Technologies, pp. 1-16, 2019, https://doi.org/10.1007/s00542-019-04549-2

[34] S. Stoukatch, F. Dupont and J. -M. Redouté, "Development of wafer singulation technique for MEMS and MOX gas sensors using 355 nm UV laser ablation process", EUROSENSORS XXXVII Conference, Wroclaw, Poland - Sept. 7th - 10th 2025, accepted for publication, in press.