Advanced wafer singulation techniques for miniaturized metal-oxide (MOX) micro-hotplates based gas analyzer

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***Abstract*— A typical process flow for micro-hotplate sensors includes the fabrication of the sensor wafer followed by functionalization. Functionalization involves the local deposition of a sensing material, or several materials in the case of a multi-gas analyzer. Functionalization makes the analyzer sensitive to specific gases. Typically, functionalization is a wafer-level process, of which screen and inkjet printing, dispensing and direct atomic layer processing are good examples. Once the sensor wafer is fully processed and functionalized, it must be singulated onto individual sensor dies. After that the individual sensor die will be assembled. Various die singulation methods have been reported, but they can pose serious problems for the functionalized sensor wafer. The sensing materials used for functionalization are dominated by metal-oxides, which are sensitive to environmental factors, including thermal exposure, humidity uptake, etc. In this paper, we reviewed various die singulation techniques and methods, in function of their suitability for singulating fully functionalized metal-oxide (MOX) micro-hotplates sensor silicon wafers, including wafer sawing, laser ablation and dicing, scribe-and-break, stealth dicing, plasma dicing, dicing before grinding and others. Finally, we identified the most suitable wafer singulation method for the selected application and presented an outlook.**

Keywords*— metal-oxide sensor assembly, wafer singulation technique, micro-hotplates sensor, back-end processing of functionalized sensors, advanced packaging

I. INTRODUCTION

Various wafer singulation methods [1] are known to singulate finished silicon (Si) wafer in individual dies. Typically, singulation is the last step for the wafer processing. The most matured technologies are widely used for singulation of IC CMOS wafers and successfully extended on MEMS wafers [2]. MEMS wafers can indeed be singulated using similar techniques as for IC wafers if their particularities are taken into account. For example, MEMS wafers with movable parts such beams, micro-mirrors bridges, RF switches etc. are typically diced unreleased and the movable parts are supported by a corresponding medium. This is because the released movable parts of an individual MEMS device can be mechanically damaged relatively easily during the sawing process, which employs high pressure water flow, and contaminated by the dicing dust generated during sawing. After the sawing, the wafer is rinsed and released (the support for the moving parts is removed), and the individual MEMS dies are ready to be integrated with corresponding ICs [3]. The majority of MEMS are integrated and assembled together with ICs [2] either using wafer-level monolithic processes, or heterogenous techniques. In this case, the wafers which are bonded together are singulated using conventional IC singulation technology.

Miniaturized MOX micro-hotplates are typically processed [4] using MEMS technology and, similarly to MEMS, can be integrated with IC CMOS wafers by wafer-level monolithic or heterogenous techniques. Unlike typical MEMS devices, MOX gas sensors have no movable parts but have a suspended micro-hotplate membrane which is only 25-50 µm thick compared to the total wafer thickness of 300 µm. Similarly to the movable features of MEMs, these membranes are fragile and sensitive to mechanical and thermally induced stresses.

The final step in CMOS-MEMS monolithic and heterogenous micro-hotplates gas sensor fabrication is so-called post-processing or functionalization. The process is performed at wafer-level and includes deposition of sensing material, or materials in case of multi-gas sensors. For this, various application methods are used, which can be divided into two large groups: thin and thick film technologies.

The basis of the sensing material depends on the specific gas sensing application and consists of various n- and p-type metal oxide semiconductors, such as SnO_2, TiO_2, WO_3, Zn0, CuO [4], CdO, In_2O_3 [5] etc. or heterostructures such as CuO/SnO_x and SnO_x/CuO for example [6].

What most sensing layers have in common is that they are sensitive to environmental factors, including thermal exposure [7], moisture absorption [8], direct contact with other substances, etc., depending on the design of the sensor and the nature of the sensing material [9]. Such factors can reduce the sensitivity and selectivity of the sensitive layer [10], cause poor repeatability, accelerated aging, reduce service life [11], increase energy consumption and, in extreme cases, can cause irreversible changes that compromise the functionality of the sensor. Therefore, the sensitive surface of the MOX gas sensor must be protected from any of the impacts mentioned above. However, after the functionalization of the micro-plates gas sensor wafer, the wafer must be singulated into individual dies.

This research was supported by: HORIZON-CL4-2023-RESILIENCE-01-33 - Smart sensors for the Electronic Appliances market (RIA). 101130159 – AMUSENS.

The wafer singulation techniques that are commonly used for CMOS ICs and MEMS are not compatible with CMOS MEMS micro-hotplates gas sensor wafers. This is because the latter wafer is not only fragile, due to the presence of the micro-hotplate membrane, but also sensitive to harsh environmental factors that occur during the wafer singulation, due to presence of the sensitive layer. An alternative singulation method must hence be adopted, based on known wafer singulation techniques or a combination of them.

This paper is structured as follows: the Introduction section raises the concern that micro-hotplates gas sensor wafers can't be processed using conventional singulation methods widely adopted for CMOS ICs and MEMS, and that alternative techniques must be used. In Section II, we review the most common wafer singulation methods used in the semiconductors industry. Section III covers the design, manufacture and application of gas sensors. Section IV proposes the most promising singulation technology for MOX gas sensors. Finally, a conclusion and outlook are given in Section V.

II. Wafer Singualtion Technology

Conventional wafer processing uses a so-called dicing after grinding (DAG) [12, 13] sequence, in which wafers are first thinned down to specified thickness and only then are diced. The wafer is thinned down in a back side grinding (BSG) [12, 13] process before it is diced. In contrast to conventional DAG sequence, there is also dicing before grinding (DBG). In DBG sequence, the wafer is first partially cut, to a depth which is greater than the final target thickness. The wafer is then thinned to the final target thickness, that results in die separation. The DAG and DBG dicing sequences are illustrated in Fig.1.

The wafer can be diced using one of these singulation techniques: sawing, scribe and break, plasma and chemical etch, various laser methods, or a combination of these methods [14].

A. Saw dicing

Wafer sawing [14] is the most mature and predominant technology for varieties of wafer singulation applications. This is a mechanical cutting method that employs a rotating spindle (typically 30,000 rpm) equipped with a diamond blade saw that is brought in direct contact (feeding speed between 5 and 100 mm/s) with the wafer to separate the latter into individual dies [15]. The width of the dicing blade, which is typically between 40 to 200 µm [16, 17], defines the width of the dicing kerf or the dicing street.

However, this process imposes several constraints that can compromise the sensing layer integrity and its performance. During sawing, the wafer is exposed to a high-pressure water flow (of so-called cooling and cutting water) directed into the dicing area, potentially affecting the entire area of the individual die. Due to the flow of water, the sensitive layer can be mechanically damaged or even washed away. Contact with the silicon dust generated during wafer sawing can also compromise the functionality of the sensing layer. In the case of an IC, such concerns can be overcome with minor measures. Meanwhile, MEMS wafers with movable features are typically diced unreleased, while the movable features are still supported. The wafer is eventually coated with an additional protective layer on the front side. After dicing, the MEMS wafer is vigorously rinsed, the protective layer is stripped and the movable parts are released.

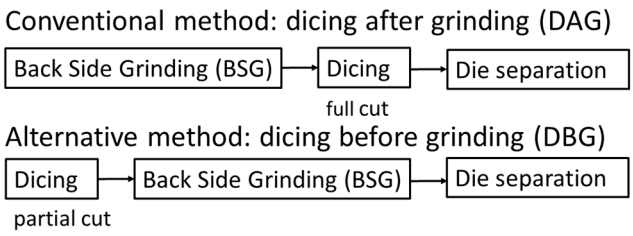

Fig. 1. DAG versus DBG dicing sequence.

The area along the kerf typically encounters some chipping, for example for a dicing blade of 40 µm wide the chipping along the kerf of 30 to 40 µm are considered acceptable [15], while on the back-side of the wafer the area affected by chipping appears larger.

A. *Scribe-and-break method*

Another potential alternative is the scribe-and-break method [18], which, unlike sawing, is a dry process and was being widely used until the early 1980s, when it has been replaced by sawing techniques due to the high sensitivity of the scribe-and-break method to crystal plane orientations and its dependence on wafer thicknesses. The method is based [19] on inducing stress in the wafer by creating a scribe line of 3-5 µm wide and 100-200 µm deep on the wafer surface, followed by fracturing the wafer along the scribe line (Fig.2). Initially, the scribe line was made with a diamond scriber. Later, in some cases, it was replaced by partial cutting with saw dicing, and eventually, with the development of laser technology, by laser ablation [20]. The first two techniques belong to mechanical scribing. The breaker bar, in some cases, is replaced by an expandable dicing tape, the tape expansion causing the singulation of the dies.

Currently, this method is primarily used in light emitting diode (LED) integration technologies and in III-V semiconductor compounds (such as GaN, InP, GaAs, GaP) [21] which are typically processed on relatively small wafers having narrow die-separation streets (2-5 µm).

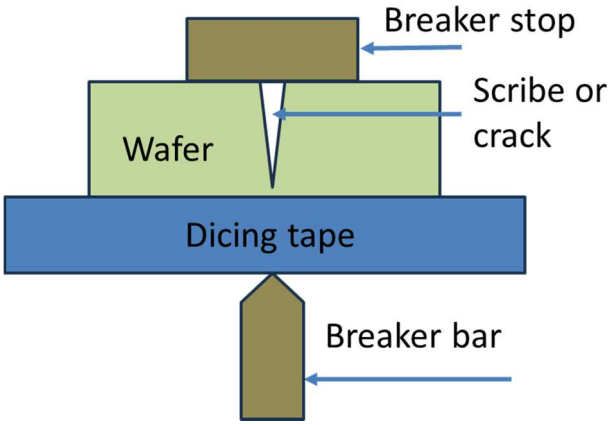

Fig. 2. Principle of scribe-and-break method

B. *Plasma dicing and Chemical etching*

As the thickness of the wafers becomes thinner [22], from a full thickness wafer of 300 µm, then down to 100 µm and 50 µm [23], and even further down to 30 µm, the wafer becomes brittle [24]. That drives an increasing demand for wafer singulation technology that doesn't require a mechanical contact between the wafer and the dicing tool. A valuable alternative to the mechanical dicing is plasma etching, often referred to as a reactive-ion etching (RIE) [25], and chemical etching.

The most common RIE technique used for the wafer singulation is deep reactive-ion etching (DRIE), which employs fluorine-based process gases SF_6 and C_4F_8 [26], Using this method, it is possible to obtain steep flawless sidewalls with spacings as narrow as 10 µm wide [27]. The narrowing of the dicing street width achieved by plasma dicing lead to an increasing number of dies per wafer. The method generates little to no stresses in the wafer compared to the conventional saw dicing technique. Other defects that often occur during saw dicing, such as chipping and cracking, are significantly decreased. Another advantage of plasma etching is the ability to create irregularly shaped cuts. The plasma etch can be employed in both [28] DBG [29] and DAG processing. The process is applied on the entire wafer and is relatively fast.

To prevent etching of the top structures of the wafer during the DRIE process, the entire surface of the wafer must be protected. For this purpose, an additional coating layer is usually required, which can be of various organic material, such as photoresist, polyimide [30], or as shown in [31], water soluble coats. These protective coatings are then removed after dicing. They can also take the form of a permanent etching mask applied on the entire surface of the wafer and sequentially patterned accordingly to develop the corresponding dicing street. The etching mask remains on the surface of the wafer surface after the dicing [32]. Impact of the RIE on the dicing tape must be also taken into account [33, 34]. The dry etch method has a lower environmental impact because it uses gaseous agents rather than liquids as in the wet etching process.

The wet etching process typically uses CMOS compatible etchant tetramethylammonium hydroxide (TMAH) or, in some cases where CMOS compatibility is not required, potassium hydroxide KOH [31]. The process like the dry etch requires an etching mask. The wet etching results in a sloped sidewall that increases the width of the kerf. The dicing streets are larger as for the wet etching. There are ongoing efforts to create steeper vertical walls and reduce the width of the dice street. For example, the authors of [35] developed a catalytic wet etching method that uses a combination of a noble metal catalyst and hydrofluoric acid (HF) as an etchant. Using this method, they processed vertical trenches 150 µm deep and less than 8 µm wide. At the same time, wet processes are more accessible because they do not require special equipment.

C. *Laser dicing*

Laser dicing is a method of singulating a silicon wafer into individual dies by means of a focused laser beam. Currently, this is the main alternative to the well-proven and matured saw dicing, over which it has a number of advantages. Due to the narrow laser beam diameter (5-15 µm) [36], laser cutting results in narrow kerf widths and less damage and chipping [37]. This method provides faster cutting speeds (up to 10 times faster) compared to saw dicing. Unlike other cutting methods, such as saw dicing and scribe-and-break methods, which cut only in a straight line, the laser can achieve almost any cutting line, including irregular shapes. The laser dicing uses fewer consumables compared to other methods. The process is completely non-contact, during which no mechanical load is applied on the wafer. Silicon laser cutting itself does not require water and is a completely dry process. However, in some laser cutting processes and setups, water can help cool the wafer and reduce contamination.

However, laser dicing relies on the interaction of a laser beam with the material being processed, and the physics of this interaction still needs to be well understood and the practical application of this method is complicated by the various physical interactions that are taking place [38]. The main parameters influencing these interactions are the laser wavelength, pulse duration, beam shape and diameter, and material feed rate.

According to the mechanism of interaction of the laser beam with the material, laser cutting can be divided into two large groups: laser ablation and stealth dicing.

1) Laser ablation dicing

During laser ablation (Fig. 3), the laser beam is focused on the cutting surface of the wafer. The result is that the cut starts at the top of the wafer and runs towards the bottom of the wafer. There are 3 main approaches to laser ablation dicing, namely: laser grooving, laser scribing and laser full-cut. Typically, laser grooving is a silicon singulation technique where cut quality is critical and any defects such as chipping, layer delamination, etc. need to be avoided or significantly reduced. For that reason, the wafer is first grooved by a laser, and then fully cut by saw dicing. Scribing comprises cutting shallow grooves or trenches, then breaking by applying a mechanical load, similar to the scribe-and-break process. Finally, laser full-cut implies to make a complete cut into the silicon wafer. This process works well for thin wafers of 50–100 µm thickness. For wafers in this thickness range, due to their fragility, laser ablation is superior to dicing and scribe and break techniques. However, for thicker wafers which require a higher pulse energy, laser ablation becomes less effective due to potential local overheating in the cutting area and material melting and sublimating, causing debris and damage.

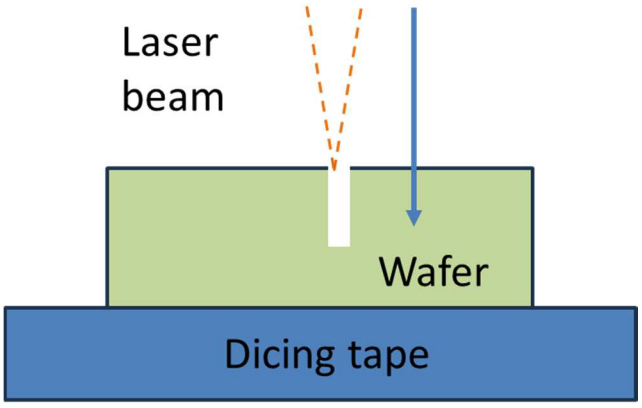

Fig. 3. Principle of laser ablation dicing.

Laser ablation as a singulation technique for silicon wafers is described in many scientific publications and technical notes. There are several recent review papers in which the authors examine different laser techniques [39] for processing silicon wafers, including different UV-lasers [40] with wavelengths of 193 nm, 248 nm, 343 nm, and others. Paper [41] examines different lasers including a 355 nm UV-laser for dicing silicon wafers. Reference [42] reports on micromachining 0.18 mm and 0.60 mm thick silicon wafers using a 355 nm UV-laser.

Despite this, the technology is commercialized only by a limited number of companies. For example, Disco Corporation, Japan, developed the Disco DFL 7160 Laser Dicer [43] for wafer ablation and the DFL7362 Laser dicer [44] for Stealth Dicing™. Those systems were developed by a joint venture between Disco and Hamatsu Photonics, Japan [45]. More information on the stealth dicing is given in Section II.D.2. The DFL7161 performs full cuts for silicon and compound semiconductors wafers. The DFL7362 is a fully-automatic laser dicer for 300 mm diameter wafers, used mainly to singulate ultra-thin silicon wafers. Silicon wafers with a thickness of 50 µm or less can be singulated at high speed while maintaining a high die mechanical strength. In principle both of them can perform thin wafer cuts up to 50 µm thick. On the official Disco web-site there is no direct information about which laser (type and wavelength) are integrated in these dicers. According to [46], the authors used a Disco DFL7160 laser dicer equipped with a 355 nm UV laser to process 45 nm CMOS Cu low-k silicon wafers with a thickness of 280 µm and a diameter of 300 mm. A dicing width of 120 microns has been achieved in this way.

Another commercially available laser dicing system is developed by Synova, Switzerland. The LDGS 300A is a fully automatic laser dicing and edge grinding system. It is suitable for dicing, edge-grinding, drilling and slotting of wafers. The system, in its standard configuration, is equipped with a diode pumped solid state Nd: YAG pulsed laser, with a wavelength of 355/ 532 nm [47]. Various laser sources (Green, UV, IR) [48] can be integrated into LDS systems to address future challenges.

Another manufacturer of dicing equipment, Accretech, presented the ML301 EXWH, a laser cutting machine for wafers with a diameter of up to 300 mm, on the company's official website [49]. However, according to the same website, production and sales of the ML300 series have been temporarily discontinued.

To conclude the section on the laser ablation, the laser system including UV lasers are a valuable alternative to the wafer saw technique [50]. Laser ablation dicing is a quick process and result in narrow dicing street. However, such laser dicing has several limitations related to the depth and the width of the dicing cut [51]. It is very problematic to perform a full cut on a 300 µm or thicker thinned wafer [52]. There are two main ablation regimes with low and high laser fluence [37, 39, 40]. For the low laser fluence regime, the laser process is mainly photochemical and there is no obvious molten areas [40]. However, this process is slow and there is maximal etching depth that can be achieved. In order to cut thicker silicon layers, a higher laser fluence is used, that results in local overheating [40]. That causes different dicing defects, such as debris formation due to redeposition of evaporated or sublimated material. Protecting the wafer surface can reduce these effects, but it is an additional processing step that increases the processing cost and reduces the benefits of the dry nature of laser processing. Another consequence of local overheating is thermal damage in the form of an increase in the heat-affected zone (HAZ) and chipping. The quality of the laser cut, and the corresponding damage induced on the wafer during laser processing must be taken into account. That being said, laser ablation works very well [53] to perform shallow cuts such as 20-200 µm [54] that can work for separating thin wafers (50-150 µm or less) or as a complementary technique used in combination with other methods requiring a partial cut [55, 56].

2) Stealth laser dicing

In stealth laser dicing [57] (Fig. 4), the laser beam, unlike for the laser ablation process, creates internal micro damage throughout the depth of the wafer. Forced expansion of the wafer, initiated by the expanding wafer tape on the back of the wafer, causes separation of the wafer in individual dies. The process provides a narrow kerf of 1-3 µm wide [58]. The laser process involves a short laser pulse duration that does not cause melting, sublimation, or excessive heating of the surrounding material. There is no chipping, debris or thermal damage that typically occurs during the laser ablation process [59] and no silicon dust as in dicing, or in the scribe-and-break process. There is no need for water cooling and rinsing, as it is a completely dry process. The stealth laser dicing method proves highly effective on smooth surfaces and on silicon wafers with a certain electrical resistivity and doping levels. Difficulties may arise when cutting rough surfaces, dicing streets with high doping content or high resistivity, and through metallization [60].

A. Summary of wafer singulation technologies

To summarize this section: sawing dicing is an all-purpose process and predominant for singulation of IC wafers, while the scribe-and-break technique is used for special applications such as singulation of fragile or hard compounds. Both processes are the most mature and cost effective. They have a high throughput and a flexible setup. Laser (laser ablation and stealth dicing) and plasma dicing are dry processes, and are typically used where special constrains are imposed, such a specific demands for dry processing, and/or a high quality outcome, such as a narrow kerf, reduced mechanical stresses, limited chipping, steep sidewalls etc. Such processing is generally more expensive than sawing and is used when the importance of meeting specific requirements outweighs the overall cost. A number of quality-critical applications require a combination of the techniques described above [61].

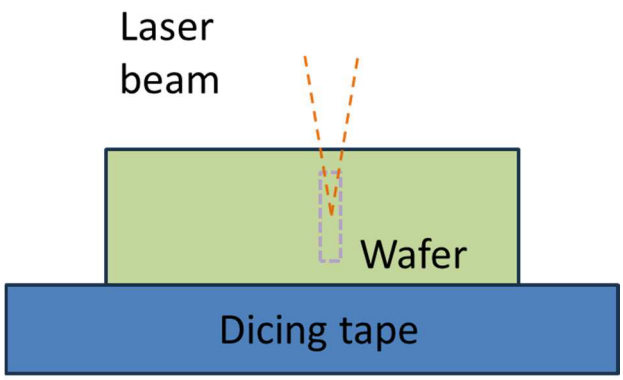

Fig. 4. Principle of stelth laser dicing.

In order to select an optimal singulation method, suitable for a particular wafer, the wafer must be analyzed in function of its capability to withstand the exposure to specific stresses encountered during the singulation process. In the section below, we will discuss the features of a MEMS micro-hotplate plate gas sensor wafer and how these influence the process of selecting the most suitable separation method.

III. METAL-OXIDE (MOX) MICRO-HOTPLATES GAS SENSOR

MOX gas sensors are becoming dominant in indoor and outdoor air quality monitoring to meet health, safety and environmental requirements. They are used in a large variety of applications including domestic appliances, HVAC, automotive, industrial and environmental monitoring. They usually target the detection of gases related to people's safety. Among these are the well known carbon monoxide and dioxide (CO and CO_2), and varieties of volatile organic compounds (VOCs) such as benzene, formaldehyde, nitrogen dioxide etc., that can be found in offices or in a domestic setting. These gases can originate from human activities or artificial sources within their respective environments. . Other gases such CH4 or H2 [62] for example, can be also found at domestic level or in cars due to leaks and by uncontrolled release. The WHO [63] classified important air pollutant and theirs associated risks to human health.

MOX gas sensors commonly use mature semiconductor technologies, such as MEMS, because of the requirement of miniaturization and low power consumption. As a result of that, these sensors are low cost, miniaturized, and supplied to customers in the form of surface-mount technology (SMT) devices. They exhibit also disadvantages that are mainly related to the MOX layer stability causing reduced measurement accuracy, degraded repeatability and sensitivity to non-target gases, and they are influenced by temperature and humidity. According to Yole forecast [64] gas sensors market was worth $1.3 billion in 2023, and it will reach $2.1 billion in 2029 with an increase of 8% in value compared to 2023.

MOX micro-hotplates gas sensors are typically processed [4] using MEMS technology and, similarly to MEMS, can be integrated with IC CMOS wafer by wafer-level monolithic or heterogenous techniques. Currently, the manufacturing of gas sensors is dominated by the monolithic process, depicted in Fig. 5, while the heterogeneous integration process is based on a bonding sequence in which fully processed CMOS and MEMS IC wafers are mechanically and electrically connected together to form a complete system.

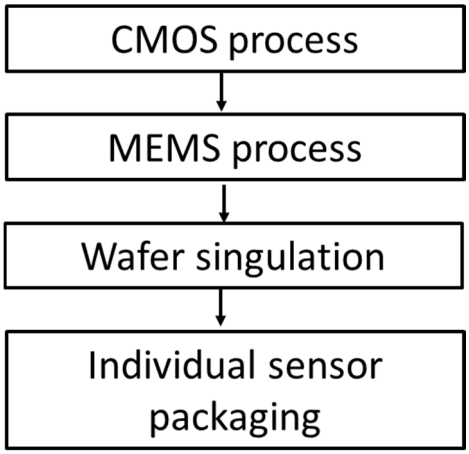

Fig. 5. Monolitic MOX micro-hotplates gas sensors manufacturing process.

During the monolithic process, once CMOS processing is completed, the corresponding MEMS sequence includes processing a membrane, deposition and patterning of the heating element, applying the insulation layers and the read-out electrodes. The configuration of the membrane and corresponding sensing layer(s) enables single- or multi-gas sensing functionality [65]. The structure of the micro-hotplate is presented in Fig. 6.

Depending on the design of the sensor, the membrane (Fig. 7) can be partially sealed off, suspended or in the form of a bridge or inter-digitated electrodes (IDE) [66].

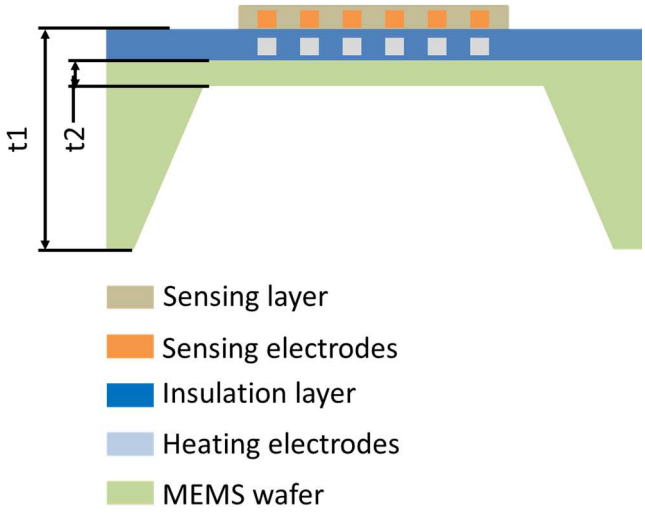

Fig. 6. Cross-sectioning view of MEMS wafer with micro-hotplates and sensitng layer. Where t1 and t2 are thicknesses of MEMS wafer and micro-hotplate membranes.

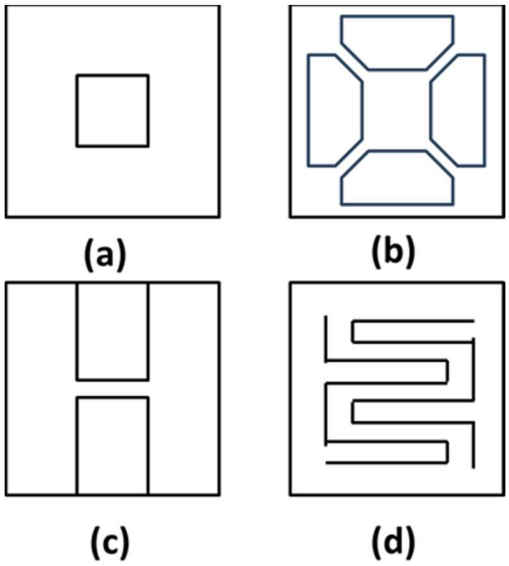

Fig. 7. Top view of micro-hotplate membranes with various configurations: (a) closed membrane, (b) suspended membrane, (c) bridge form membrane, (d) IDE.

The membrane is typically 25-50 µm thick, which is very thin compared to the total wafer thickness of the MEMS wafer (around 300 µm). The membrane is processed by backside cavity etch, via deep reactive-ion (DRIE) [67] or by wet etching processes using potassium hydroxide (KOH) [68] or tetramethylammonium hydroxide (TMAH) [69]. All of these processes, except the KOH process, are CMOS compatible, but the DRIE process provides steep sidewalls that can help reducing in-plane dimensions of the sensor. At the same time, wet processes are more accessible because they do not require special equipment.

The membrane must be as thin as possible to minimize the contact area between the micro-hotplates and the wafer, in order to reduce the heat flux transferred to the die and therefore the power consumption. Typical operating temperature of MOX sensors are in the range of 200 to 450°C [11], while CMOS ICs must not be exposed to temperatures above 300°C. On the other hand, the thinner the membrane, the more fragile it is, and a correct balance must be found between membrane thickness and energy consumption. For example, [70] reports on a miniaturized low-power MOX gas sensor processed at the wafer-level on 390 µm-thick silicon wafers with a sensing area reduced to 100 ×100 µm² using DRIE . Its power consumption is less than 20 mW at 300°C. Apparently, the thick-film gas-sensitive layer applied using the drop-coating method provided additional robustness to the miniaturized microheater without significantly increasing power consumption [70].

The final step in CMOS-MEMS monolithic and heterogenous micro-hotplates gas sensor fabrication is so-called post-processing or functionalization. The process is performed at the wafer-level and includes deposition of sensing material or materials in case of multi-gas sensors. For this, various application methods are used, which can be divided into two large groups: thin and thick film technologies. Among the thin film technology methods, the most common are physical, chemical or a combination of both, vapor deposition (P/CVD), atomic layer deposition (ALD), and magnetron reactive sputtering [4]. Such methods are well known and compatible with CMOS and MEMS fabrication platforms. Thick film technology is rapidly emerging, typical examples are spray, drop and spin coating, and screen, aerosol-jet and inkjet printing, etc. Thick film methods require post-MEMS processing. The sensing layers are dominated by metal-oxides and, in the case of thick-film technology, it also includes additional components such a binder for example.

Most sensing layers are sensitive to environmental factors, including thermal exposure [9], moisture absorption [10], direct contact with other substances, etc., depending on the design of the sensor and on the nature of the sensing material. This is due to the inherently sensitive nature of the system, where the target gas interacts with the surface of the sensing layer, causing changes in resistance or other parameters of the MOX layer. This imposes specific requirements for the surface of the sensing layer, meaning that it must be kept free from any uncontrolled substances and not exposed to any factors that could alter the condition of the surface. Such factors affecting the sensing element can reduce the sensitivity and selectivity of the functional layer [6], cause poor measurements accuracy and repeatability, accelerated aging of the functional layer, reduced service life of the sensor [7], and increased energy consumption. In extreme cases, this can cause irreversible changes in the sensing layer that compromise the functionality of the sensor.

Therefore, the sensitive surface of the MOX gas sensor must not be exposed to any of the factors mentioned above or, if it is not possible, it must be protected from these adverse influences. For example, to protect the MOX sensing layer, the authors of [70] introduced a gas-permeable membrane applied at the wafer level to seal the MOX layers, resulting in a simplified packaging process. However, after the functionalization of the micro-plates gas sensor wafer, the wafer must be singulated onto individual dies using known wafer singulation methods as described in Section II, this process bears specific risks to the sensing layer functionality.

IV. OUTLOOK AND CONCLUSIONS

Obviously, not all methods mentioned and analyzed in Section II are suitable for singulation of a fully functionalized metal-oxide (MOX) micro-hotplates multi-gas sensor silicon wafers. Therefore, the most common singulation method, the conventional wafer dicing by sawing, cannot be applied on a fully functionalized MOX sensor wafer because it uses process water which can eventually affect the performance of the MOX layer due to its sensitivity to environmental factors. The microheater on the released wafer being unsupported during the sawing can also be damaged by the high pressure water flow. Dry processing methods, such as the scribe-and-break, do not have this disadvantage. Meanwhile, the scribe-and-break method can not only contaminate the sensor with the silicone scribing dust but, most likely, cause a breakage not along the scribe line, but in the mechanically weakest part of the sensor, namely the micro-hotplate membrane.

Non-contact methods such as etching can be a good alternative to this. However, this method is not without its drawbacks. Interactions between etchants and the MOX layer during the plasma or wet etching process can pose a risk to the integrity and performance of the MOX sensing layer. Laser ablation and stealth laser dicing are two dry processes

that also do not require mechanical load can be considered as good candidates for the singulation of MOX micro-hotplates gas sensor wafers: however, the process flow must be carefully designed taking into account the limitations associated with each process. In this case, a possible process would involve thinning the wafer to a thickness that can be easily processed by the chosen laser method, and then performing separation of the wafer with an appropriate laser.

Another possible way out of this is to process the entire wafer before applying the MOX layer, then singulating the wafer and then performing functionalization of the wafer as a final processing step. In this case, a singulated wafer of individual sensor dies attached to a dicing tape becomes incompatible with sequential thin film deposition which is required during MOX application when using a CMOS or MEMS technology platform. An alternative to this is to apply a MOX layer using post-MEMS processing such as thick-film technology. However, most of these are serial processes, unlike MEMS processing which is applied at the wafer level and is only suitable for the selected MOX composition.

ACKNOWLEDGMENT

The work was fully funded by the European framework program HORIZON-CL4-2023-RESILIENCE-01-33 - Smart sensors for the Electronic Appliances market (RIA), 101130159 – AMUSENS. This review paper was inspired by consortium members during the preparation of the AMUSENS project.

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